Inaugural Lecture Series 142

BEFORE THE DAWN OF MOLECULAR ELECTRONICS

By

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OWO UNIVERSITY PRESS LIMITED

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An Inaugural Lecture Delivered at Oduduwa Hall
Obafemi Awolowo University Ile – Ife, Nigeria
On Tuesday July 11, 2000

Inaugural Lecture Series 142

Obafemi Awolowo University Press, Limited Ile-Ife, Nigeria.

ISSN 0189-7845

Printed by
Obafemi Awolowo University Press Limited,
Ile-Ife, Nigeria.

INTRODUCTION

Today, civilization has passed the threshold of the second industrial revolution. The first industrial revolution which was based upon the steam engine, enabled man to multiply his physical capacity to do work. The second industrial revolution, which is based upon semiconductor (or solid-state) electronics, is enabling man to multiply his intellectual capabilities. In other words, what technology has done to the world to modernise it is what solid-state electronics is doing to technology. Ultra large scale integration (ULSI) electronics, as it is presently termed, is the most advanced state of semiconductor electronics, and represents a remarkable application of scientific knowledge to the requirements of technology. In this lecture, we will highlight the past and present stages of development of this science and technology and elucidate the trend for the future of what is becoming a giant scale integration electronics. In addition, we will highlight Nigeria's position in the acquisition of this technology and proffer the way forward.

Electronics, by definition, *is that field of science and engineering that deals with electron devices and their utilisation*. An electron device is one in which conduction is principally by electrons moving through a vacuum, gas or semiconductor. In elementary science, we say matter is made up of gas, liquid or solid. Electrically, the solid can be classified as a conductor, a semiconductor or an insulator. This lecture will deal, in the main, with the art, science and technology of semiconductor devices fabrication. Having said this, I must be quick to add that semiconductor devices cannot be fabricated in the absence of the conductor and the insulator. Neither will it be possible to fabricate semiconductor devices without the

use of liquids and gases. What we are, therefore, dealing with here is an encompassing materials science with a special emphasis on semiconductor devices.

The Pioneer Electron Device - The Vacuum Tube

The pioneer electron devices were vacuum tubes (also known as thermionic valves). The basic vacuum tube was the vacuum diode. The diode consists of an evacuated glass envelope which contains two electrodes known as the anode and cathode. The two electrodes are usually cylindrical in shape with the cathode in the centre and the anode surrounding it. The cathode is heated indirectly by a filament wire and the emitted electrons are attracted by the positive potential applied to the anode. Diodes were used for various applications ranging from very small diodes for the demodulation of radio waves to the very large devices for power rectification . The vacuum diode was invented by Ambrose Fleming in 1902.

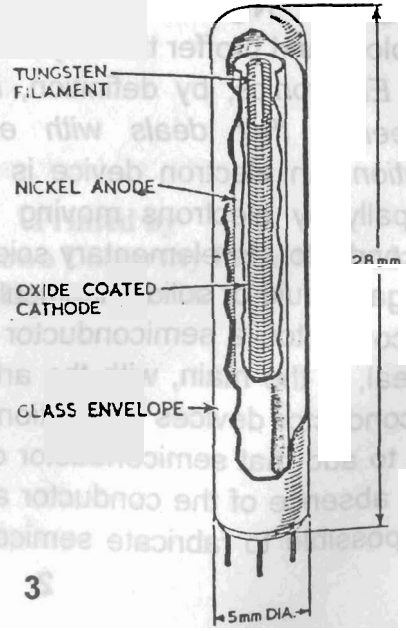

Fig. 1
Typical miniature thermionic diode, Mullard type EA76. Reverse voltage before breakdown, 420V. Maximum forward current, 9mA. Reverse current, virtually nil. Filament ("heater") voltage, 6.3V.

Figure 1 shows a typical vacuum diode of the miniature type - the Mullard EA76. In 1907, Lee de Forest invented the audion tube or the triode. In addition to the above two electrodes, the triode has a third electrode (the control grid) between the anode and the cathode

The triode is used for applications such as amplification, oscillation, mixing, etc. The main limitation of the triode occurs at high frequencies due to interelectrode (anode-grid) capacitances (the Muller effect) and transit time effects. The limitations of the triode were overcome by inserting a further grid (screen grid) between the control grid and the anode, thus the tetrode was invented. However, the characteristic of the tetrode has a negative resistance portion which from the point of view of amplification is a disadvantage. The negative resistance has, however, a practical value in that it is used to sustain an oscillator circuit. The negative resistance characteristic of the tetrode was largely eliminated by inserting a further grid (the suppressor grid) between the screen grid and the anode. The five-electrode tube was known as a pentode and was used extensively in voltage and power amplification because they produce low distortion.

The vacuum tubes (diode, triode, tetrode and pentode) were used in the pioneer radio receiver and TV sets. We remember the Philips and Pye receiver sets of the 40s and 50s. You switch them on and after a few seconds, you see the glowing vacuum tubes, then follows the sound from the receiver speaker. These earlier devices (tubes) were robust but power consuming and hence inefficient . However, they were reliable and worked. In the early 1960s, the vacuum tube became an endangered specie as solid - state or semiconductor electronics matured from infancy. By the late '70s, the vacuum tubes became museum pieces. There is,

however a class of specialized vacuum devices which has refused to become museum pieces. These are mainly the display devices. In electronic systems, information is often displayed visually as signal wave forms or pictures. The most commonly used devices are the cathode ray tube and the television tube. These will continue to be in use until the flat screen liquid crystal displays (LCD) are well developed to replace them. Other vacuum devices still in common use include the X-ray and the transmitter tubes.

The Semiconductor or Solid - State Era

Semiconductors are a group of solid materials with values of the electrical resistivity at room temperature generally in the range ~ 10^{-2} - 10^{9} ohm-cm, intermediate between good conductors (metals) (10^{-6} ohm-cm) and insulators (~10^{14} - 10^{22} ohm-cm). It is significant that the conductivity of these materials can be varied over wide ranges by changes in temperature, optical excitation and impurity content.

Semiconductor materials are found in column IV and neighbouring columns of the periodic table. The column IV semiconductors, Silicon and Germanium, are called elemental semiconductors because they are composed of single species of atoms. In addition to the elemental materials, compounds of column III and column V atoms (e.g. GaAs), as well as certain combinations from II and VI (e.g. CdS) and also from IV and IV (e.g. SiGe, SiC), make up the intermetallic, or compound semiconductors. In addition, in the last few years, some ternary and quaternary semiconducting materials have been subject of investigation.

Among the numerous semiconductor materials, Si is used for the majority of devices; rectifiers, transistors and integrated circuits are usually made of Si. The compounds are used most widely in optoelectronic devices (i.e. those requiring the emission or absorption of light). For example, semiconductor light emitters are commonly made of such compounds as GaAs, GaP, and mixed compounds such as GaAsP. Fluorescent materials such as those used in TV screens usually are II-VI compound semiconductors such as ZnS. Light detectors are commonly made with InSb, CdSe, PbTe and PbSe. Si and Ge are also widely used as infrared and nuclear radiation detectors. An important microwave device, the Gunn diode, is usually made of GaAs. The wide range of semiconductor materials offers considerable variety in properties and provides a lot of flexibility in the design of electronic functions.

The dramatic invention of the transistor (a solid-state or semiconductor device) in 1948 by Bardeen, Brattain and Shockley caused a revolution in electronics. This device was small, less than 5% of the size of a typical vacuum tube, consumes very little power and hence efficient. Above all, the transistor does practically everything that the vacuum tube could do. The pioneer (1948) transistor was of the 'mesa' type.

The IC or planar devices era

The first planar transistor was produced in 1959 at the Fairchild Laboratories in the USA. Originally, all electronic devices were discrete units existing as separate entities within their own packages. The work of Noyce in 1958 gave rise to the technology which made it possible to create many devices

arranged as a complete electrical circuit on a piece, or chip of semiconducting material; thus opening a new era of integrated circuits (IC) or microelectronics. Following the production of the pioneer planar transistor in 1959, the first few ICs were produced in early 1960s' and in 1964, standard ICs with 32 components were produced. This component density was doubled in 1965.

Observation of this modest beginning of ICs led Gordon Moore in 1965 to predict the doubling of density of components per IC at regular time interval (yearly initially). It is amazing that this Moore law (as it is now known) still holds, more or less, today. Therefore, as the technology matured, increasing number of devices could be integrated to form increasing number of complex circuits. The levels of integration with approximate chronology are given below:

1. Early 1960s': SSI (small scale integration), a few tens of components per circuit of 1cm. by 1cm. in area.
2. Late 1960s': MSI (medium scale integration), several hundred components per circuit.
3. Late 1970s': LSI (large scale integration), a few thousand components percircuit.
4. 1980s': VLSI (very large scale integration), several tens of thousand components per circuit.
5. 1990s': ULSI (ultra large scale integration), several million components per circuit

Solid-state electronics, perhaps more than any other field of technology has enjoyed an explosive development in the last four decades. Large scale integration produces circuits which are smaller, faster, more reliable and cheaper. How do

we achieve higher levels of integration? We make the devices smaller and pack them more densely. This miniaturisation of components, starting with the invention of the transistor, makes them much more susceptible to particle contamination, hence the need for the use of cleanrooms.

Today, manufacturers of semiconductor circuits have become the largest users of cleanrooms. The reason is that the manufacturing operations take place at almost the molecular level and the physics of the operation of the device depends upon the purity of the materials in atomic percentages measured down to parts per trillion. These levels are unheard of in any other human endeavour.

CLEANROOMS

The development of the first cleanrooms for industrial manufacturing largely started during the 2nd world war in the USA and the UK mainly in an attempt to improve the quality and reliability of instrumentation used in guns, tanks and aircraft. It was realized that cleanliness of the production environment had to be improved or such items as bomb sights and precision bearing would malfunction. At that time, cleanrooms were built which copied hospital operating room design and practices. However, it was soon appreciated that 'bacteria-free' was not the same thing as 'particle-free'. A great deal of effort was therefore put into ensuring that materials and surfaces did not generate particles but it was not fully appreciated that airborne dispersion of large quantities of particles by machine and human beings had to be removed by large quantities of pure air. The production of high efficiency particulate air (HEPA) filters and the realization of the

'unidirectional' or 'laminar flow' concept of ventilation at the Sandia Laboratories, Albuquerque, New Mexico, USA, help further development of cleanrooms.

A cleanroom has a special meaning and it is defined by the US Federal Standard 209 as:

> "A room in which the concentration of airborne particles is controlled to specified limits"

and in the British Standard 5295 as:

> "A room with control of particulate contamination, constructed and used in such a way as to minimise the production, generation and retention of particles inside the room and in which temperature, humidity and pressure shall be controlled as is necessary"

Classification of Cleanrooms

Cleanrooms are classified by the cleanliness of their air. The method most easily understood and universally applied is the US FS 209 in which the number of particles equal to and greater than 0.5 micron is measured in one cubic foot of air and this count is used to classify the room. This classification is shown in Table 1.

Table 1: A Simplified US FS 209 Classification of Cleanrooms

FS 209 Classification	1	10	100	1000	10000	100000
No. of particles/ft^3 <0.5 microns	1	10	100	1000	10000	100000

The required standard of cleanliness of a room is dependent on the task performed in it. The more susceptible the product is to contamination, the better the standard. Table 2 gives an indication of the task carried out in different classification of cleanrooms.

Table 2: Possible Cleanroom Requirement for Various Tasks

Class 1	IC manufacturers developing submicron or nanoscale geometries
Class 10	Semiconductor manufacturers producing VLSI circuits with line width less than 2 μm
Class 100	IC manufacturers
Class 1000	Manufacture of high quality optical equipment. Assembly of miniaturised bearings and precision gyroscope
Class 10000	Assembly of precision hydraulic or pneumatic equipment, servo-control valves, precision timing devices, high grade gearing
Class 100000	General optical work, assembly of electronic components, hydraulic or pneumatic assembly

DEVELOPMENT OF Ics

For many years, silicon has been the main semiconductor of the integrated circuit industry. Two primary advantages have made silicon the material of choice for microelectronic circuits. First, it is easily oxidised, and the resulting oxide film is both an excellent insulator and an effective barrier during implantation and diffusion of dopants into the patterned regions of the silicon substrate. Second, low-defect, large-diameter crystals can be readily grown, enabling manufacture of wafers up to 8 inches (20 cm) in diameter at a reasonable cost.

The structure of an IC is quite complex both in the topography of its surface and in its internal composition. Each element in such a device has an intricate three-dimensional architecture that must be reproduced exactly in every circuit.

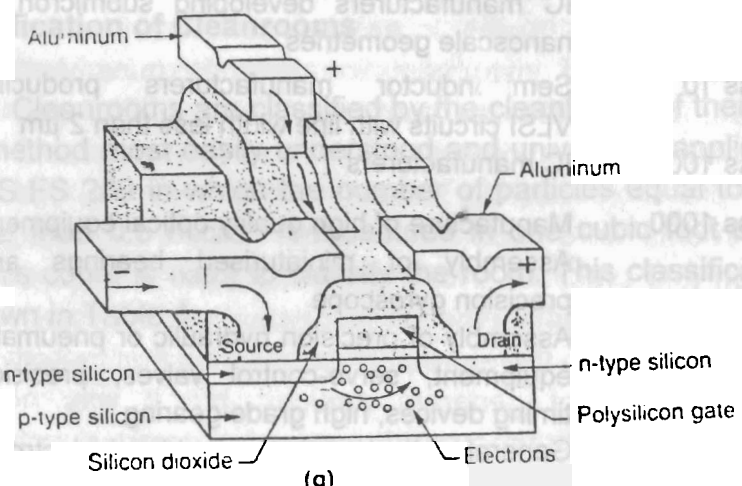

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Figure 2Schematic representation of a single transistor cell.

Figure 2 is a schematic representation of a single transistor cell (within an IC). The structure is made up of many layers, each patterned in a manner required by the circuit design. Some of the layers lie within the substrate semiconductor wafer and others are stacked on top. Fabrication of an IC therefore, requires processes for depositing and patterning this sequence of layers.

Construction of the individual circuit elements requires modification of the electrical properties of the semiconductor substrate, which is accomplished by the selective diffusion of tiny amounts of impurities into specific regions of the substrates that have been defined by lithographic processes. These individual circuit elements are electrically isolated or connected both internally and externally with patterned layers of insulating and conductive films, respectively. Typical thin film materials encountered include such materials as silicon dioxide, polysilicon, and aluminium. Fabrication of the three-dimensional circuit geometries characteristic of a complete metal-oxide semiconductor (MOS) or bipolar device (transistor) may require as many as 25 individual patterning steps.

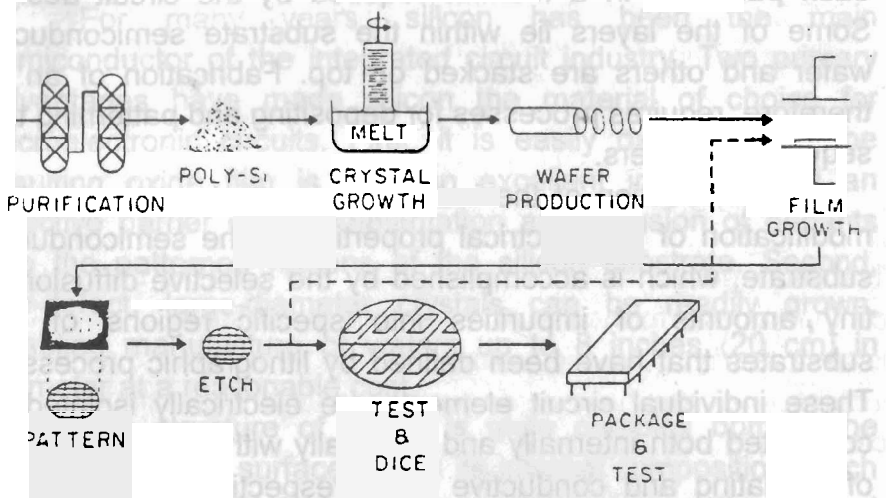

Figure 3 Process sequence in the production of integrated circuit devices.

Figure 3 shows an outline of the manufacturing sequence of a large scale integrated circuit. Common practice divides the manufacturing of ICs into three phases; material, wafer fabrication, and assembly and test. We will give below a brief summary, together with the level of contamination control required, of the manufacturing steps used in making semiconductor circuits. The VLSI and the CMOS (complementary MOS) process on silicon are used as illustrative examples.

Table 3: Materials

Starting with silica sand, the process is as follows:

	Start with	Into	Produces
a	Sand, coal, coke, wood chips	Submerged arc electric furnace at 2000°C	Metallurgical grade Si. (MGS) - 98% Si
b	MGS (powdered) + HCl(gas) + catalyst	Reactor at 300°C	$SiHCl_3$-impure (trichlorosilane)
c	$SiHCl_3$ (impure)	Distillation column	$SIHCl_3$ - pure
d	$SiHCl_3 + H_2$	Reactor	Electronic grade Si (EGS) - 99.9999%
e	EGS	Cz crystal grower at 1450°C + Inert gas (Ar) atmosphere	Single-crystal silicon ingot
f	Single crystal Si ingot	Special grinder	Polished cylinder with flat(s) - full length to def. xtal orientation
g	Polished cylinder	Diamond saw	Round slices with 1 or 2 flat sides
h	Slices	Grind, lap & polish machines	Wafer ready to be made into ICs

It must be pointed out that the above processes in most cases now, constitute a whole industrial set-up on its own. Therefore, device manufacturers purchase their starting material (silicon

wafers) from such vendors. During the above sequence, most of the operations take place in an ordinary factory environment. Protection against contamination is provided, for most part, by doing the processing within sealed systems. Preparation of the charge for the Czochralski (Cz) puller, however, as well as clean-up of the crucible, must be done in a well-controlled cleanroom (minimum standard Class 100). Any contamination introduced during that step will get into the ingot and cause failure in the process to make a single crystal or cause unacceptable electrical properties to develop. Process h also requires the cleanest of environments (min. Class 100) to allow the equipment to produce the required finish, thickness and flatness. Also great care must be taken to avoid leaving any mobile ions or doping elements on the surface. Subsequent high temperature operation could then diffuse these into the crystalline structure and destroy the desired electrical properties.

As indicated in process d, attainment of 100% purity for the EGS is not possible. This is due to the segregation constant of some very difficult impurities, especially the heavy metals, which has made them impossible to eliminate. This fact has some implications for devices fabrication as we shall see later on

Wafer Fabrication

In this phase of manufacturing, all of the active and passive elements of the semiconductor circuits are built onto or into the polished silicon wafer. On the microscopic level, one can observe a cross-section of pure silicon being changed by: addition (diffusion) of impurity atoms deep into the pure

wafer to a controlled depth and concentration; layers of silicon oxide being deposited over everything; then selectively etched away; a different type of impurity atoms is added (diffused) into the etched windows again to a controlled depth; this is followed by another layer of oxide. The process is repeated for as many as 23 times (for a MOS circuit), interconnected, stabilised, passivated etc.

Processes here include; heat up to 1100°C; attack by exceptionally aggressive chemicals; flooding with chemical vapour so toxic that the most rigorous controls are required to protect workers; exposure to violent levels of ionising radiation and superheated, ionised plasmas. All of these take place to create circuits and devices whose dimensions range down to 0.25 μm for critical features. The active elements which are interconnected into one device can be in the millions. All of these are packed into a chip measuring no more than one centimetre square. As all the dimensions are controlled by photographic processes (photolithography), the success or failure of manufacturing is absolutely determined by the control (and elimination) of contamination. The minimum Class required is 100, with the most critical steps requiring class 1 (based on 0.1 μm particles).

Table 4: Wafer Fabrication

The process encountered in wafer fabrication are:

	Start with	Into	Produces
a	Polished wafer	Diffusion furnace or epitaxial reactor (at high temp, with dry or wet O_2 gas)	Wafer with SiO_2 layer on surface
b	Oxide covered wafer	Spiner-coater which applies photoresist (PR)	Wafer with oxide + PR layers
c	Wafer with PR	Pattern application (exposure of PR to UV light thro' photomask)	Exposure of pattern on PR
d	Exposed wafer	Developer (wash out either exposed or unexposed pattern depending on type of PR	Wafer with PR pattern
e	Wafer with PR pattern	Etch (etchant removes oxide exposed by pattern development)	Silicon exposed through oxide + some PR
f	Windowed wafer + PR	PR removal (either plasma or wet etch removal)	Clean windowed wafer ready for processing
g	Windowed wafer	Diffusion furnace or ion implant (add impurities to exposed silicon)	Implanted or diffused pockets in Si

n	Diffused clean wafer	Repeat steps b to g (steps b to g can be repeated many times with different photomasks - depending on the complexity of the circuit)	Wafer with clean surface
i	Clean wafer	Sputter reactor or vacuum evaporator (apply Al coating)	Wafer with conducting layer
j	Metallised wafer	Repeat steps b to f	Clean wafer with required conducting patterns
k	Clean wafer with surface conductors	Reactor (nitride overcoat application)	Surface protected wafer
l	Surface protected wafer	Back etch (for thinning)	Thinned wafer
m	Thinned wafer	Backside plating	Electrical contacts

The above sequence serves to illustrate the complexity and enormous number of steps required. This sequence or part of it may be repeated up to 23 times for one device. The complexity is added to by the precise inspections, measurement and cleaning required at least once between steps.

In the wafer fabrication area, the objective of contamination control is to protect the work-in-process from errors created by contamination. There is a rule of the thumb which says that the maximum size of particle which can be tolerated is one tenth the dimension of the smallest critical feature. For example, an electrical gate whose smallest critical dimension is 1.0 μm can be made defective by a particle 0.1 μm and larger. Other types and sources of contamination, such as dissolved contaminants in deionised water can produce killer defects that may or may not be traceable. For the above reasons, in the wafer fabrication area, the utmost contamination control must be extended to the work until the wafer is completely protected. Above all, all the materials (gas, water, chemicals etc.) used in this phase must be of electronic grade.

Assembly and Test

This third phase is where individual devices are tested, separated from others on the wafer, mounted onto a substrate header or leadframe, electrically connected from the terminating pads on the silicon chip to the leads on the leadframe, encapsulated, finally tested and shipped. In general, cleanliness levels between Class 100 and 10,000 are required.

Table 5: Assembly and Test Processes

The operation in this phase are as follows:

	Start with	Into	Produces
a	Completed wafer	Multi-point prober (function test of each device)	Tested wafer. Failed devices identified with ink dots
b	Tested wafer	Mounting fixture (wafer mounted on plastic mount on metal ring)	Wafer ready for dicing saw
c	Mounted wafer	Dicing saw (diamond saw precisely cuts thro'wafer to separate dies.)	Separated die adhesively held to plastic
d	Separated die	Die bonder (vacuum probe picks off good dies and attaches them to leadframe)	Die on leadframe
e	Device on leadframe	Lead bonder (gold wire attachment of device to leads)	Device electrically attached to leads
f	Electrically completed device	Encapsulating (either plastic moulding or hermetically sealed can)	Completed device ready for final test
g	Completed device	Burn-in test (prolonged test under operating conditions and environmental extremes)	Device ready for shipment

The needs for contamination control in this phase are very different from the other two previously described manufacturing processes. Here the device is already protected from atomic and ionic pollutants, but must still be protected against large conductive particles shorting between leads. Also they must be protected against electrostatic charge build-up and discharge (in this region, the devices are very vulnerable, a 12 volt discharge can destroy a circuit). Any oil or other material on surfaces may prevent sealing or adhesion of plastic or ink. Films or particles on a surface may also interfere with obtaining a good electrical contact and cause false reading on tests. The principal difference is in the size or quantity of contaminants. In the wafer fabrication area, contaminants that are too small to be seen in an inspection microscope may be fatal. The opposite is true in assembly and test; the fatal particles or other contaminants may be too large to be readily picked up in the microscope or other inspections.

THE O. A. U. (ILE-IFE) CLEANROOM PROJECT

One of the major thrusts of the Department of Electronic and Electrical Engineering, Obafemi Awolowo University, Ile-Ife, is to gear its research efforts toward the technological development of Nigeria. One of the results of this effort is the establishment of the Solid-state Electronics Laboratory in 1973. Activities in this laboratory thus has its main theme as technology acquisition and development with appropriate fundamental research as an important back-up in line with the traditional role of a University Academic Department.

The Ife cleanroom project started due largely to the foresight, hardwork and able leadership of Prof. V. A. Williams, who I call the 'father' of electronics in Nigeria. Necessary

equipment and facilities were acquired for installation in room 118 of the Department of Electronic and Electrical Engineering which became our cleanroom. Setting up a cleanroom facility in our dust laden environment was not an easy task. In addition, being the first of its kind in this sub-region, we ran into a number of infrastructural problems and a lot of adaptation had to be carried out in order to surmount such problems. Installation, calibration and operational activities started in earnest and devices (passive and also silicon based) fabrication processes commenced there after.

Work was usually bugged down by inadequate supply of water (this was before the Opa dam came into existence) and electrical power failure. Here is a technology that requires uninteruptible and clean water and power supplies apart from an adequate supply of water at some optimum pressure for cooling purposes. Some modification and adaptation had to be carried out on our facilities in order to cope with these two major problems. I will highlight just 2 examples of these modifications here.

First, for an adequate supply of cooling water, we had to create a water reservoir out of the gutter behind the Physics block. Rain water was collected and stored in this 'reservoir'. Water from this source was pumped into a tank on the roof of the building and then allowed to run under gravity back into the reservoir through our vacuum system, diffusion pumps and furnaces for cooling purposes. This served as a 'close-circuit' water supply system. With time we were confronted with a problem of low water pressure on the supply line. As a result, the diffusion/oxidation furnaces and diffusion pumps could not function optimally. Despite the installation of an additional pump to boost water supply from the roof, the problem persisted. We eventually traced the cause to a small toad

which was sucked into our water supply system through the intake pipe from the reservoir. The toad managed to survive until it got into the equipment supply pipe where it gave up, thus partially blocking the pipe. To eliminate toads and tadpoles etc., we had to mount some filter on our inlet pipe.

Secondly, frequent power failures had a tremendous damaging effect on our furnaces apart from destroying materials undergoing processing in the furnace when the failure occurs. When a furnace operating at a temperature of 1100°C experienced a power failure, one would watch helplessly as the cooling fans melted and dropped one after the other under the intense heat of the furnace ambient. Of course, any work in progress in such a furnace when the power failure occurred is only good for the dustbin. Following repeated power failures, a d.c. to a.c. converter was built and incorporated into the furnace system electronics. This converter, which comes on automatically following a power failure, kept the fans running for a period of time long enough to ensure a safe temperature level in both the tube and associated control compartments.

To date, we have acquired the technology for the production of both passive and active electronic components. Methods have been developed in our laboratory for the fabrication of;

(i) Composition resistors by formation of composite carbon-plastic compounds.
(ii) Thin film resistors by vacuum evaporation.
(iii) Thin film resistors by cathodic sputtering. The sputtering equipment was designed and constructed by this lecturer.
(iv) Transistors by the planar technology

Resistors were fabricated for the first time in this laboratory in 1975 while bipolar junction transistors were produced in 1979. With this feat, the technological know how and know why for the production of ICs were practically attained. I remember a colleague heaved a sigh of relief after one of our successful production runs, saying : 'despite the invasion of toads in our cooling water system and myriads of problems, we were able to produce active devices in the tropics of Africa'. Our products have been exhibited on a number of occasions. Government personnel (both military and civilian) have visited our facilities to see for themselves. Apart from the usual admiration of the products and facilities, requests for support to keep the development work going is yet to be entertained. That some of our equipment are still functioning in the face of lack of fund, is due largely to the level of commitment and ingenuity of the personnel attached to the laboratory.

SOME CONTRIBUTION TO DEFECT ENGINEERING IN SEMICONDUCTORS BY THE LECTURER

Defects have always played a double role in semiconductor device technology; there are both wanted and unwanted defects or impurities. The device performance fundamentally relies on intentionally introduced defects in the bulk, e.g dopant impurities for p-n junctions, and at interfaces, e.g. Metal Oxide Semiconductor (MOS) structures. Likewise, point defects are indispensable for standard processing steps, e.g. diffusion, oxidation and contact formation. On the other hand, defects generated at elevated processing temperatures, cannot be reduced to their thermal equilibrium concentrations

due to slow reaction kinetics. In addition, metal contaminants or implantation damage can be deleterious to subsequent processing and device performance, affecting leakage current, gate oxide integrity and yield. The unparalleled development of semiconductor technology has, therefore, been fundamentally enabled by defect engineering.

As stated earlier, attainment of 100% purity for EGS rods and therefore wafers is not possible. This is mainly due to the segregation constants of some very difficult impurities, especially the heavy metals which render them impossible to eliminate and are, therefore, present in the as grown silicon. These elements, which include Fe, Cr, Cu, Ag, Mn, Ni, Ti, V, Co, Li, etc. are hence generally inherent in EGS wafers which are the starting materials for devices fabrication. In addition, some of these unwanted impurities may be inadvertently introduced into the wafer during cleaning or high temperature processing. They (contaminants) are generally known to diffuse mainly by the interstitial mechanism in Si substrate and ultimately degrade device performance by introducing multiple deep levels which act as traps or recombination centres. A detailed understanding of the diffusion mechanism and electrical properties of these unwanted impurities and hence of their possible control in silicon wafers are, therefore, of prime importance for attaining improved yield in Si devices.

The technological importance of removing harmful metal impurities from the active areas of device has stimulated research on various gettering techniques. The major methods employed include phosphorus diffusion, ion implantation and intrinsic or internal gettering by means of oxygen precipitation. The lecturer has, in conjunction with some colleagues, investigated the diffusion, some electrical properties and the intrinsic gettering of a number of these impurities in the silicon

substrate.

Our modest contribution which have appeared in various international journals include studies on the following impurity elements; Ag (Adegboyega *et al.* 1996, 1996a); Cr (Adegboyega and Poggi, 1991, 1991a); Cu (Adegboyega and Poggi, 1991a, 1991b, 1994); Fe (Adegboyega *et al.* 1989, 1990); Mn (Adegboyega, Osasona and Susi, 1997) in the silicon wafer from which we have drawn the following conclusions:

- All the elements studied diffuse by the interstitial mechanism in the silicon substrate. While most will remain in the interstitial site, a high percentage of Fe and Cu atoms will precipitate on quenching from high temperature. Fe, in particular, has a tendency to diffuse, even at room temperature. Fe and Cr do form FeB and CrB pairs with boron acceptors of p-type Si substrates
- Electrically, all the above impurities behave as donors except Mn and Ni which are amphoteric (i.e. they are both donors and acceptors)
- They are all lifetime killers in the silicon device, i.e., they give rise to many deep but different energy levels in the silicon substrates.
- While Cr and Mn are easy to getter, Fe, Cu and Ag are very difficult.
- Our work has shown clearly that there is a relationship between intrinsic gettering efficiency and the reaction of impurities with the interstitial oxygen of the substrate on one hand and also on the amount of precipitated oxygen.

These conclusions have various significant implications for the semiconductor industry.

This lecturer has also made considerable contribution to defect engineering in the second most important semiconductor material (i.e. GaAs). Our work on the out-diffusion of Cr from GaAs substrate (B. Tuck *et al*, 1979) showed convincingly that a small amount of Cr impurities from a semi-insulating substrate material find their way into the epitaxial layer grown on the substrate thus resulting in poor characteristics for devices fabricated in such a layer. This finding carries a lot of implications for the GaAs FET technology and was partly instrumental to the incorporation of a buffer layer between substrate and epitaxial layers by GaAs devices manufacturers. In 1979, Tuck and Adegboyega showed that the diffusion of Cr in GaAs is a complex interstitial mechanism and thus paved the way for a better understanding of the important Cr:GaAs system. Tuck and Adegboyega in 1980 employed the radio-tracer techniques and electrical measurements to show that Ag diffuses in GaAs by means of an interstitial - substitutional mechanism, eventually occupying the Ga sites. This work also showed that Ag is a p-type impurity most probably a double acceptor in GaAs.

Using photoluminescence measurements on Cr - diffused GaAs, Adegboyega and Tuck (1981, 1983) showed that Chromium exists in more than one ionisation states in GaAs and that complexes involving lattice atoms could also be formed with Cr impurities in Chromium - doped GaAs.

Thermal conversion of semi-insulating GaAs into p-type semiconducting materials was a problem that GaAs devices manufacturers had to grapple with in the 70s and 80s. Adegboyega in 1983 showed conclusively that this problem is dependent on such processing parameters as temperature and time of anneal and also that Ga and As vacancies play important roles in the process of thermal conversion and the

culprit acceptors was linked, for the first time, to antisite Ga atoms.

CONTRIBUTION TO THE DEVELOPMENT OF PHOTOVOLTAICS

Electricity can be generated directly from sunlight by means of the photovoltaic (PV) effect. Devices that use the PV effect to generate electricity are called solar cells and they are made from semiconductor materials. These cells where developed during the 1950s and they proved to be the best power source for extra-terrestrial (space) missions. Satellites need a source of electrical energy that will last for a long time without any attention. All conventional batteries will run down after a period of time. The solar cell, however, will continue to deliver electric power as long as sunlight is available. In the mid 1970s, efforts were initiated to make solar cells for terrestrial applications. Terrestrial applications of solar cells include; provision of electricity for areas remote from electric grid, powering of communication repeater stations, water pumping for irrigation and drinking purposes, etc.

Essentially, all of solar cells used for both space and terrestrial applications have been made of junction diodes. However, being an area dependent device, the silicon solar cell is, at today's cost, too expensive for terrestrial application when compared to conventional sources of energy. To reduce the cost of this class of solid state devices, non-silicon cheaper materials may have to be found or device structures other than p-n junction developed for the silicon based cells. These alternatives are currently receiving the attention of various researchers. Cuprous oxide, Cu_2O, is a material that can

provide cheap cells. Adegboyega in 1985 deviced a simple process for the growth of Cu_2O on copper substrates. He also developed a process for the separation of unwanted CuO (an insulator) from the semiconducting Cu_2O (Adegboyega 1990). The MIS (metal-insulator-semiconductor) solar cell structures have the potential for combining ease of fabrication with low cost and hence are also suitable for large scale terrestrial conversion of solar energy. Generally, a lot of research has been carried out on the I and S components of this structure. However, more work is required on the semi-transparent metal layer before efficient, stable MIS devices can be fabricated. In 1987, Adegboyega reported the spectral and thickness dependence of the transmittance as well as the sheet resistance of vacuum-deposited semi-transparent films of aluminium and correlated the variations in their spectra and resistances with modifications of the deposit due to oxidation process encountered in the laboratory atmosphere. A model describing the kinetics of the oxidation process was subsequently provided (Adegboyega 1989).

EVOLUTION FROM MICRO- TO NANO- ELECTRONICS

The driving force for the progress of integrated circuit technology has been the demand for ever increasing speed and integration level by the computer industry. The key approach to meeting these demands has been scaling, i.e., the reduction of the feature sizes of the elementary IC components. After more than two decades of relentless scaling to ever smaller dimensions for higher packing density, faster circuit speed, and lower power dissipation, CMOS (complementary MOS) technology has become the prevailing

technology for ULSI application today. These advances have led to computers and networks with far superior performance and dramatically reduced cost per function.

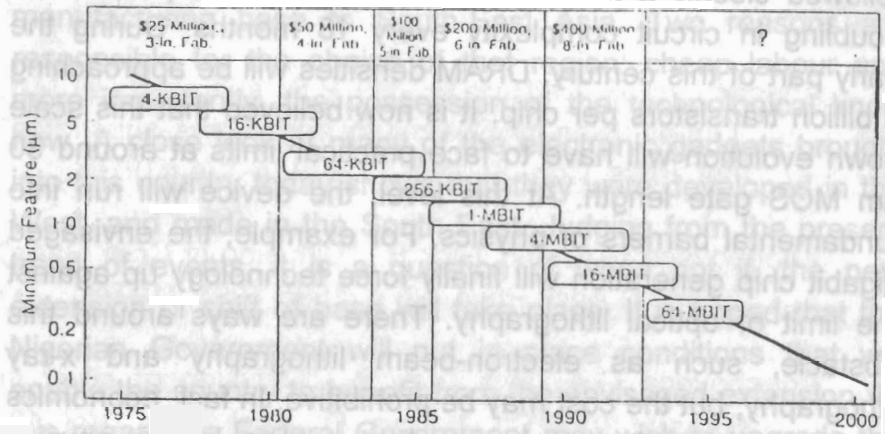

Figure 4 Minimum feature size in metal oxide semiconductor DRAM device as a function of the year the devices were first commercially available, the level of integration, and the Fab-line cost.

Figure 4 shows the exponential decrease of minimum feature length, i.e., gate width, junction depth and gate oxide thickness of MOSFET (MOS field effect transistor) structures with time. The rate of about 13% reduction per year has led to the current 0.25 μm CMOS technology with 0.15 μm channel length being used in the manufacturing of the 1- Gb DRAMs (dynamic random access memory) and 800-Mhz microprocessors with the number of transistors per chip in the 10^7-10^8 range. It must be pointed out that DRAMs and microprocessors are basically CMOS transistors. CMOS devices of 0.1 μm (100 nm) channel length have been fabricated in research laboratories. Scaling of CMOS into the

sub 0.1 μm brings it into the nanometer or nanoelectronics classification. [Note that I nm is approximately 10 atomic diameters].

For 25 years, microprocessors and DRAMs have followed closely a revised Moore's law, which stipulates the doubling in circuit complexity every 18 months. During the early part of this century, DRAM densities will be approaching a billion transistors per chip. It is now believed that this scale down evolution will have to face practical limits at around 30 nm MOS gate length. At this level, the device will run into fundamental barriers of physics. For example, the envisaged gigabit chip generation will finally force technology up against the limit of optical lithography. There are ways around this obstacle, such as electron-beam lithography and x-ray lithography, but the cost may be prohibitive. In fact, economics may constraint Moore's law or limit scaling before physics does. At present, researchers are still learning to exploit more the properties of semiconductors and production processes. But, at some point, this technology - like all others - will stop growing exponentially and enter the realm of diminishing marginal returns. Below the 30 nm MOS gate length, innovative devices, probably, based on quantum mechanical effects or molecular electronics may have to emerge.

Well, so far electronics has evolved into microelectronics and the dawn of nanoelectronics is here. At this point in time, however, we can rule out the possibility of evolution to acronyms such as picoelectronics, femtoelectronics etc. but only time will tell what the next generation of electronic devices will look like.

CONCLUSION

Mr. Vice-Chancellor, sir, in concluding this lecture, I would like to note that presently, the major semiconductor devices manufacturers have extended, if not shifted, their manufacturing base to South-East Asia. Two reasons are responsible for the choice of that region; cheap labour and more importantly, the possession of the technological know how. A close look at many of the electronic gadgets brought into this country today shows that they were developed in the West, and made in the South East. Judging from the present trend of events, it is a question of when not if, the next extension or shift of base will take place. It is hoped that the Nigerian Government will put in place conditions that will enable the country to benefit from the envisaged extension. In this regard the Federal Government may wish to upgrade the semiconductor laboratory in the Department of Electronic and Electrical Engineering, Obafemi Awolowo University, Ile-Ife, to the status of a National Semiconductor Centre. To the best of my knowledge, this laboratory is the only place in this sub-region where there is a nucleus of the semiconductor device manufacturing technology. Apart from training the required man power, the Centre will, with a minimum of effort, embark upon a small scale manufacturing of some electronic components. I must admit, however, that venturing into such a rapidly evolving field as solid-state electronics, without an adequate back-up research outfit, by a developing country like Nigeria has its hazards, most notably a frighteningly quick obsolescence. Nonetheless, we would find it impossible to take off technologically as all technology now solely depends on solid-state electronics. We should now be avoiding the acronym: developed in the West, made in the East and sold

(or consumed) in Africa (third world).

I thank you for your attention, may God bless you.

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